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Amdt. dated 9/12/06
Reply to Office action of 6/13/06

CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and

listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended). A test circuit for testing a

memory circuit, the test circuit comprising:

a data input line for providing test data to be written to

the memory circuit;

a comparator unit connected to said data input line and to

the memory circuit, said comparator unit comparing expected

values received over said data input line with the test data

read from the memory circuit, the test data previously having

been written to the memory circuit over said data input line;

and

a data change circuit connected between said data input line

and the memory circuit, said data change circuit being

controllable depending on a result of a comparison performed

in said comparator unit such that when an error occurs,

further test data can be written to the memory circuit in a

manner altered by said data change circuit;

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said data change circuit passing the test data in an

unaltered form to said memory circuit if no error occurs and

passing the test data in an inverted form to said memory

circuit if an error occurs.

Claim 2 (original). The test circuit according to claim 1,

wherein the expected values correspond to the test data

previously written to the memory circuit.

Claim 3 (original). The test circuit according to claim 1,

wherein:

said data change circuit is one of a plurality of data change

circuits; and

said data input line is one of a plurality of data input

lines each connected to one of said data change circuits,

said data change circuits being controlled by said comparator

device such that when the error occurs in a memory area

addressed through one of said data input lines, each of said

data change circuits is controlled such that the further test

data on said plurality of data input lines can be written to

the memory circuit in the altered manner.

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Claim 4 (currently amended). ~~The test circuit according to~~

~~claim 1, wherein~~ A test circuit for testing a memory circuit,

the test circuit comprising:

a data input line for providing test data to be written to

the memory circuit;

a comparator unit connected to said data input line and to

the memory circuit, said comparator unit comparing expected

values received over said data input line with the test data

read from the memory circuit, the test data previously having

been written to the memory circuit over said data input line;

and

a data change circuit connected between said data input line

and the memory circuit, said data change circuit being

controllable depending on a result of a comparison performed

in said comparator unit such that when an error occurs,

further test data can be written to the memory circuit in a

manner altered by said data change circuit;

said data change circuit ~~has~~ having a controllable exclusive-

OR gate which, depending on a control signal generated by

said comparator device, passes the test data in unaltered

form to the memory unit or inverts the test data with an aid

of an exclusive-OR function resulting in the further test

data being altered test data.

Claim 5 (original). The test circuit according to claim 3,

further comprising a plurality of blocks each having a

plurality of further data input lines connected between said

comparator unit and the memory circuit, when the error occurs

in the memory area addressed by one of said further data

input lines of one of said blocks, said data change circuits

for all of said further data input lines of a respective

block are controllable such that the further test data on

said further data input lines of said respective block can be

written in the altered manner to the memory circuit.

Claim 6 (original). The test circuit according to claim 1,

wherein said comparison unit has a reset input for driving

said comparison unit to not alter the test data in said data

change circuit.

Claim 7 (currently amended). A method for testing a memory

circuit, which comprises the steps of:

transmitting and writing test data to a memory area resulting

in written-in test data;

reading-out the test data from the memory area resulting in

read-out test data;

comparing the written-in test data to the read-out test data;

determining an occurrence of an error if the written-in test

data differs from and the read-out test data; ~~and~~

transmitting further test data after a detection of the

error, the further test data being altered during writing to

the memory area resulting in altered test data being written

into the memory area such that a subsequent comparison of the

altered test data read out and the further test data yields a

difference; and

passing the test data to the memory area in an unaltered form

if no error occurs, and passing the test data to the memory

area in an inverted form if an error occurs.

Claim 8 (original). The method according to claim 7, which

further comprises writing the altered test data into at least

one further memory area after the detection of the error in

the memory area, so that the further test data transmitted

for the memory area and for the at least one further memory

area and the altered test data read therefrom are different.

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Claim 9 (original). The method according to claim 7, which further comprises altering the further test data into the altered test data with an aid of an exclusive-OR function after the detection of the error.

Claim 10 (original). The method according to claim 7, which further comprises altering a specific operating parameter of the memory circuit between repeated writing-in and reading-out of the altered test data.

Claim 11 (original). The method according to claim 7, which further comprises:

performing a plurality of write/read operations; and

outputting error data to an evaluation unit, the error data specifying differences between the further test data transmitted during a last write operation and the altered test data read out during a last read operation.

Claim 12 (new): A method for testing a memory circuit, which comprises the steps of:

transmitting and writing test data to a memory area resulting

in written-in test data;

reading-out the test data from the memory area resulting in

read-out test data;

comparing the written-in test data to the read-out test data;

determining an occurrence of an error if the written-in test

data differs from and the read-out test data;

transmitting further test data after a detection of the

error, the further test data being altered during writing to

the memory area resulting in altered test data being written

into the memory area such that a subsequent comparison of the

altered test data read out and the further test data yields a

difference; and

passing the test data in unaltered form to the memory area or

inverting the test data with the aid of an exclusive-OR

function resulting in the further test data being altered

test data, depending on the comparison.